BHAVANA SRIPRIYA MADDU

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OBJECTIVE

Looking for full-time opportunity in RTL / IP/ SoC Design Verification and Validation.

EDUCATION

Portland State University, Oregon, USA **Sep 2022 – June 2024**
Master of Electrical and Computer Engineering **CGPA: 3.5/4.0**
Coursework: Pre-silicon validation, post-silicon functional validation, Low power digital IC design, Assertion-Based Verification, Formal Verification, Microprocessor System Design, ASIC Modeling and Synthesis, System Verilog, Verilog Workshop, Computer Architecture.

R. V. R & J. C College of Engineering, Andhra Pradesh, India **Aug 2017 – May 2021**
Bachelor of Technology., Electrical and Computer Engineering **CGPA: 8.5/10**
Coursework: Digital Logic Design, Data Structures through C++, Microprocessors and microcontrollers, Digital Communication, Computer Organization, Computer Networks, HDL programming, Operating Systems, VLSI Design, Embedded Systems.

TECHNICAL SKILLS

Hardware Description Languages: Verilog, System Verilog

Methodology: Universal Verification Methodology (UVM)

Tools: Siemens Model Sim, Siemens Questa Sim, Xilinx Vivado, SAT solver, Synopsys Tool

Debugging Tools: Siemens Visualizer

Operating Systems: Windows, Linux

Skills: Functional Verification, Gate Level Simulation, Building modular, reusable testbenches, implementing coverage-driven verification, and leveraging transaction-level modeling in system Verilog, Very-Large-Scale Integration

Concepts: Verilog, System Verilog Design & Verification, Self-checking testbench, Exhaustive testing, Constraint Randomization, Constraints, Mailbox, Coverage, ASIC verification flow, OOPS, SAT Solver, Formal verification methods, Linear Temporal Logic, Computation Tree Logic, Symbolic Simulation, Sequential Equivalence Checking, Formal Equivalence Checking, DRAM, Cache, Cache Coherence, Virtual Memory, Assertion Based Verification methods.

WORK EXPERIENCE

Siemens EDA (Siemens Digital Industries Software), Wilsonville, Oregon, U.S.A

Associate Application Engineer **July 2024 – Present**

- **Mastering Industry-Standard Verification Tools**: Develop expertise in Questa and Visualizer, focusing on industry-standard verification practices.
- **Design and Verification**: Create and verify RTL models using Verilog, ensuring they are synthesizable and running gate-level simulations to validate functionality.
- **Advanced UVM Testbench Development**: Transition initial testbenches into fully featured UVM-based environments, enhancing test coverage and modularity.
- **Verification IP Integration**: Gain proficiency in using verification IPs to streamline testbench development and ensure robust verification.
- **Customer Support and Problem-Solving**: Leverage technical skills and tool knowledge to diagnose and resolve customer issues, providing efficient, reliable solutions.

Siemens EDA (Siemens Digital Industries Software), Wilsonville, Oregon, U.S.A

Applications Engineering Intern **Sep 2023 – May 2024**

- Training on the Simulation platform Siemens' Questa products Questa Sim and Questa Visualizer, with the Global Support division (Functional Verification) to provide post-sale technical support to meet customer needs which helps customers design and debug complex hardware and software systems, with Siemens' Questa products.
- Got hands-on experience with a project on Verilog, system Verilog design and verification.
- Developing Knowledge-Based Articles by the end of the Internship Program.

Lucid VLSI Institute, Remote

Course on Verilog and Digital Design **Dec 2022 - Feb 2022**

Training and Hands-on experience in Verilog and Digital Design. Applied concepts like Verification flow, Self-Checking testbench, Randomization, Synchronous FIFO, Verilog Design and Verification.

ACADEMIC AND INTERNSHIP PROJECTS

- **Design and verification of a synthesizable Reverse Polish Notation Calculator (Verilog, System Verilog, UVM based testbench)**

  Designed an FSM-based Reverse Polish Notation (RPN) calculator with essential sub-modules. Synthesized the design using Xilinx Vivado, producing a netlist for gate-level simulation, and verified functionality with a UVM-based testbench environment. Utilized Questa Sim for simulation and Visualizer as a debugging tool, applying coverage-driven testing and constrained-random verification to ensure functional accuracy.
- **Design and Verification of an Asynchronous FIFO (System Verilog, UVM based testbench)**
  Developed and verified an asynchronous FIFO with configurable depth and width, ensuring robustness under asynchronous conditions. Designed using System Verilog, the FIFO features independent read and write clock domains, status flags (full, empty, almost full, almost empty), and synchronized pointers. Verified functionality using a comprehensive UVM testbench environment that included custom agents, drivers, and monitors for read/write operations. Coverage analysis was conducted using built-in metrics, while results were recorded and managed through organized test cases and coverage reports.
- **Design of Synchronous FIFO with configurable Depth and width (Verilog, System Verilog, class-based testbench)**

Designed and analyzed First In, First Out design using different simulated read and write logics. It is an approach for handling program work requests from queues or stacks so that the oldest request is handled first using the Questa Sim Simulation platform and debugged using Questa Visualizer.

- **Design and Verification of an I2C-based memory subsystem (System Verilog)**
  Designed a Functional unit and connected it with the I2C master. A memory is also designed and connected with an I2c slave. Performed all kinds of memory operations using the I2C Protocol. Later, the design is also verified using System Verilog Assertions and a self-checking, exhaustive test bench.
- **Design and Verification of AES Cryptographic Algorithm (System Verilog)**
  Designed the Advanced Encryption Standard (AES) cryptographic algorithm to encrypt the plain text into a cipher text and then verified it by decrypting it into plain text using the Siemens Questa Sim Software tool.
- **Simulation of Last Level Cache (System Verilog)**
  Simulated the behavior of Last level cache for a 32-bit processor with shared memory configuration which employs a MESI protocol to ensure Cache-Coherence. Modeled communication between LLC and next higher-level cache, bus operations that LLC performs, and snoop results that LLC reports on the bus. Reported statistics on Cache misses and hits, reads, writes, and hit ratio. Prepared trace files to verify the behavior of LLC.